

DATA SHEET

MAX6352-XX

Dual voltage microprocessor supervisory IC

Product data
Supersedes data of 2003 Aug 01

2003 Oct 16

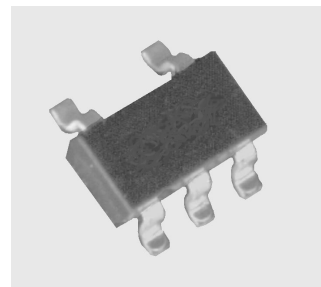
Dual voltage microprocessor supervisory IC

MAX6352-XX

GENERAL DESCRIPTION

The MAX6352-XX microprocessor (μ P) supervisory IC has dual power supply voltage monitoring in which all reset outputs are asserted when either power supply voltage falls below its preset threshold reset level. The reset state is guaranteed valid as long as either V_{DD1} or V_{DD2} is above +1 V.

The MAX6352-XX has an active-LOW debounced manual reset input and an open drain, active-LOW $\overline{\text{RESET}}$ output. It is offered in specific reset threshold levels as shown in the Voltage Threshold Levels table. The MAX6352-XX is available in the small outline 5-lead package (SOT23-5; SOP003) and operates over the extended temperature range of -40°C to $+85^{\circ}\text{C}$.



FEATURES

- Precision monitoring of multiple +1.8 V, +2.5 V, 3.0 V, +3.3 V, and +5 V power supply voltages
- Factory set precision reset thresholds
- 20 μA supply current
- 100 ms power-on-reset delay time
- Debounced manual reset input: TTL/CMOS compatible
- Guaranteed parameters over temperature
- Guaranteed $\overline{\text{RESET}}$ valid to V_{DD1} or $V_{DD2} = 1\text{ V}$

- Power supply transient immunity
- Small 5-pin SOT23 package
- Low cost, high reliability solution

APPLICATIONS

- Computers and controllers
- Portable/battery-powered equipment
- Multi-voltage systems
- Industrial and intelligent instrumentation

SIMPLIFIED DEVICE DIAGRAM

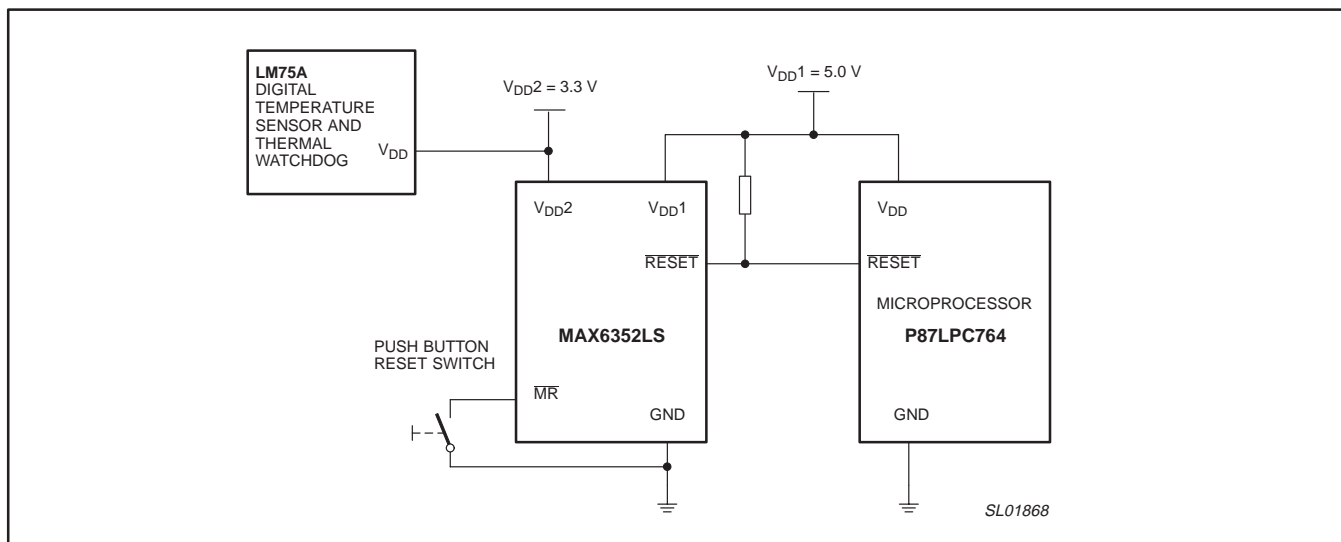


Figure 1. Simplified device diagram.

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ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | | TEMPERATURE RANGE |
|-------------|---------|---|---------|-------------------|
| | NAME | DESCRIPTION | VERSION | |
| MAX6352-XXD | SOT23-5 | plastic small outline package; 5 leads; body width 1.5 mm | SOP003 | −40 °C to +85 °C |

NOTE:

The device has 1 standard voltage output options, indicated by the **XX** on the Type Number. Additional voltage options may be available; see Table 1.

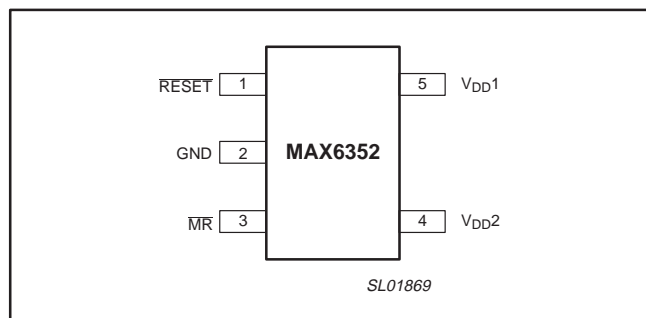
Table 1. Voltage threshold levels

| XX | V _{CC1} NOMINAL THRESHOLD VOLTAGE (V) | V _{CC2} NOMINAL THRESHOLD VOLTAGE (V) |
|---------------------------------------|--|--|
| Standard versions (note 1) | | |
| SV | 2.93 | 1.58 |
| Non-standard versions (note 2) | | |
| LT | 4.63 | 3.08 |
| LS | 4.63 | 2.93 |
| LR | 4.63 | 2.63 |
| MT | 4.38 | 3.08 |
| MS | 4.38 | 2.93 |
| MR | 4.38 | 2.63 |
| TY | 3.08 | 2.19 |
| TV | 3.08 | 1.58 |
| SZ | 2.93 | 2.32 |
| SY | 2.93 | 2.19 |
| SW | 2.93 | 1.67 |
| TZ | 3.08 | 2.32 |
| TW | 3.08 | 1.67 |
| UW | 2.78 | 1.67 |
| UV | 2.78 | 1.58 |
| RW | 2.63 | 1.67 |
| RV | 2.63 | 1.58 |

NOTES:

- Sample stock is available only in standard versions.
- Contact factory for availability of non-standard versions.

PIN CONFIGURATION

**Figure 2. Pin configuration.**

PIN DESCRIPTION

| PIN | SYMBOL | DESCRIPTION |
|-----|------------------|--|
| 1 | RESET | Active-LOW Reset Output. Open drain output configuration. |
| 2 | GND | Ground |
| 3 | MR | Manual Reset Input. Pull LOW to assert a reset. RESET is active-LOW as long as MR is LOW and remains LOW for the timeout period after MR goes HIGH. If not used connect to V _{DD1} or leave floating. |
| 4 | V _{DD2} | Supply input. Powers the device when it is above V _{DD1} and monitors its own voltage |
| 5 | V _{DD1} | Supply input. Powers the device when it is above V _{DD2} and monitors its own voltage. |

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MAXIMUM RATINGS

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|--------------------|---|------|------|------|
| V_{DD1}, V_{DD2} | Supply voltage | -0.3 | +6.0 | V |
| \overline{RESET} | \overline{RESET} output | -0.3 | +6.0 | V |
| | Input/output current, all pins | | 20 | mA |
| P | Continuous Power Dissipation (derate 7.1 mW/°C above $T_{amb} = 70\text{ }^{\circ}\text{C}$) | | 571 | mW |
| T_{amb} | Ambient operating temperature range | -40 | +85 | °C |
| T_j | Maximum junction temperature | | 150 | °C |
| T_{stg} | Storage temperature range | -65 | 150 | °C |

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ELECTRICAL CHARACTERISTICS

$T_{amb} = 25\text{ }^{\circ}\text{C}$, $V_{DD1} = V_{DD2} = +1.2\text{ V to }+5.5\text{ V}$, $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ (Note 1) unless otherwise specified.

| SYMBOL | PARAMETER | | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|---|------------|---|------|----------------------|------|--------|
| V _{DD1} , V _{DD2} | Supply voltage | | T _{amb} = 0 °C to +70 °C | 1.0 | — | 5.5 | V |
| | | | T _{amb} = −40 °C to +85 °C | 1.2 | — | 5.5 | |
| I _{DD1} , I _{DD2} | Supply current | | V _{DD1} = 5.5 V; V _{DD2} = 3.6 V; all I/O pins open | — | 20 | 50 | μA |
| V _{th1} | V _{DD1} threshold (Note 1) | MAX6352-L_ | T _{amb} = +25 °C | 4.54 | 4.63 | 4.72 | V |
| | | | T _{amb} = −40 °C to +85 °C | 4.5 | — | 4.75 | V |
| | | MAX6352-M_ | T _{amb} = +25 °C | 4.3 | 4.38 | 4.46 | V |
| | | | T _{amb} = −40 °C to +85 °C | 4.25 | — | 4.50 | V |
| | | MAX6352-T_ | T _{amb} = +25 °C | 3.03 | 3.08 | 3.14 | V |
| | | | T _{amb} = −40 °C to +85 °C | 3.00 | — | 3.15 | V |
| | | MAX6352-S_ | T _{amb} = +25 °C | 2.88 | 2.93 | 2.98 | V |
| | | | T _{amb} = −40 °C to +85 °C | 2.85 | — | 3.00 | V |
| | | MAX6352-U_ | T _{amb} = +25 °C | 2.74 | 2.78 | 2.82 | V |
| | | | T _{amb} = −40 °C to +85 °C | 2.70 | — | 2.85 | V |
| | | MAX6352-R_ | T _{amb} = +25 °C | 2.58 | 2.63 | 2.68 | V |
| | | | T _{amb} = −40 °C to +85 °C | 2.55 | — | 2.70 | V |
| V _{th2} | V _{DD2} threshold (Note 1) | MAX6352-_T | T _{amb} = +25 °C | 3.03 | 3.08 | 3.14 | V |
| | | | T _{amb} = −40 °C to +85 °C | 3.00 | — | 3.15 | V |
| | | MAX6352-_S | T _{amb} = +25 °C | 2.88 | 2.93 | 2.98 | V |
| | | | T _{amb} = −40 °C to +85 °C | 2.85 | — | 3.00 | V |
| | | MAX6352-_R | T _{amb} = +25 °C | 2.58 | 2.63 | 2.68 | V |
| | | | T _{amb} = −40 °C to +85 °C | 2.55 | — | 2.70 | V |
| | | MAX6352-_Z | T _{amb} = +25 °C | 2.28 | 2.32 | 2.35 | V |
| | | | T _{amb} = −40 °C to +85 °C | 2.25 | — | 2.38 | V |
| | | MAX6352-_Y | T _{amb} = +25 °C | 2.16 | 2.19 | 2.22 | V |
| | | | T _{amb} = −40 °C to +85 °C | 2.13 | — | 2.25 | V |
| | | MAX6352-_W | T _{amb} = +25 °C | 1.64 | 1.67 | 1.70 | V |
| | | | T _{amb} = −40 °C to +85 °C | 1.62 | — | 1.71 | V |
| | | MAX6352-_V | T _{amb} = +25 °C | 1.55 | 1.58 | 1.61 | V |
| | | | T _{amb} = −40 °C to +85 °C | 1.53 | — | 1.62 | V |
| ΔV _{th} /°C | Reset threshold temperature coefficient | | | — | 20 | — | ppm/°C |
| V _{hys} | Reset threshold hysteresis | | | — | V _{th} /500 | — | V |
| | V _{CC} to Reset delay | | 100 mV overdrive | — | 20 | — | μs |
| t _{RP} | Reset timeout period | | V _{DD1} > V _{th1} (MAX); V _{DD2} > V _{th2} (MAX) | 100 | 180 | 280 | ms |
| V _{OL} | RESET output voltage LOW | | V _{DD1} or V _{DD2} ≥ 2.7 V; I _{SINK} = 1.2 mA | — | — | 0.3 | V |
| | | | V _{DD1} or V _{DD2} ≥ 4.5 V; I _{SINK} = 3.2 mA | — | — | 0.4 | |
| | | | V _{DD1} or V _{DD2} ≥ 1 V; I _{SINK} = 50 μA; T _{amb} = 0 °C to +70 °C | — | — | 0.3 | |
| | | | V _{DD1} or V _{DD2} ≥ 1.2 V; I _{SINK} = 50 μA; T _{amb} = −40 °C to +85 °C | — | — | 0.3 | |

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ELECTRICAL CHARACTERISTICS (continued)

$T_{amb} = 25\text{ }^{\circ}\text{C}$, $V_{DD1} = V_{DD2} = +1.2\text{ V to }+5.5\text{ V}$, $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ (Note 1) unless otherwise specified.

| SYMBOL | PARAMETER | | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--------------------|-------------------------------------|---------------------------|---|-----------------------|------|-----------------------|------|
| Manual Reset Input | | | | | | | |
| V _{IL} | \overline{MR} input voltage | MAX6352-L_, MAX6352-M_ | V _{DD1} > V _{th1} (MAX) | — | — | 0.8 | V |
| V _{IH} | | | | 2.3 | — | — | V |
| V _{IL} | | MAX6352-_Y | V _{DD1} > V _{th1} (MAX) | — | — | 0.3 × V _{DD} | V |
| V _{IH} | | | | 0.7 × V _{DD} | — | — | V |
| | \overline{MR} pull-up resistance | | | 32 | 63.5 | 100 | kΩ |
| t _{MR} | \overline{MR} minimum pulse width | | | 1 | — | — | μs |
| | \overline{MR} glitch rejection | | | — | 100 | — | ns |
| t _{MD} | \overline{MR} to Reset delay | | | — | 0.1 | — | μs |

NOTES:

1. Overtemperature limits are guaranteed by design and are not production tested.
2. The reset output is guaranteed to be in the correct state if either V_{DD1} or V_{DD2} is within its specified window of operation.
3. The reset output is asserted if either V_{DD1} or V_{DD2} falls below its associated threshold voltage.

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TECHNICAL DISCUSSION

The MAX6352-XX microprocessor (μ P) supervisory IC provides system protection by monitoring two power supply voltages and asserting a reset signal if either supplies falls below the specified threshold (see Figure 3). The MAX6352-XX has an active-LOW open drain output. The output reset state is guaranteed to remain valid as long as either V_{DD1} or V_{DD2} is above +1 V. Power for the MAX6352-XX is sourced from whichever is the higher voltage: V_{DD1} or V_{DD2} .

Threshold levels

All available power supply input voltage threshold level combinations are indicated in Table 1, "Voltage threshold levels".

Manual Reset

The manual reset input, \overline{MR} is active-LOW logic. It allows the \overline{RESET} to be asserted by a pushbutton switch. A mechanical pushbutton switch is effectively debounced by the glitch filter. The typical glitch rejection is 100 ns. \overline{MR} may be driven from an external logic circuit since it is TTL/CMOS compatible. The minimum \overline{MR} input pulse is 1 μ s for $V_{DD1} = V_{DD2} = +1.2$ V to +5.5 V. When not in use, the pin is left floating or tied to V_{DD1} .

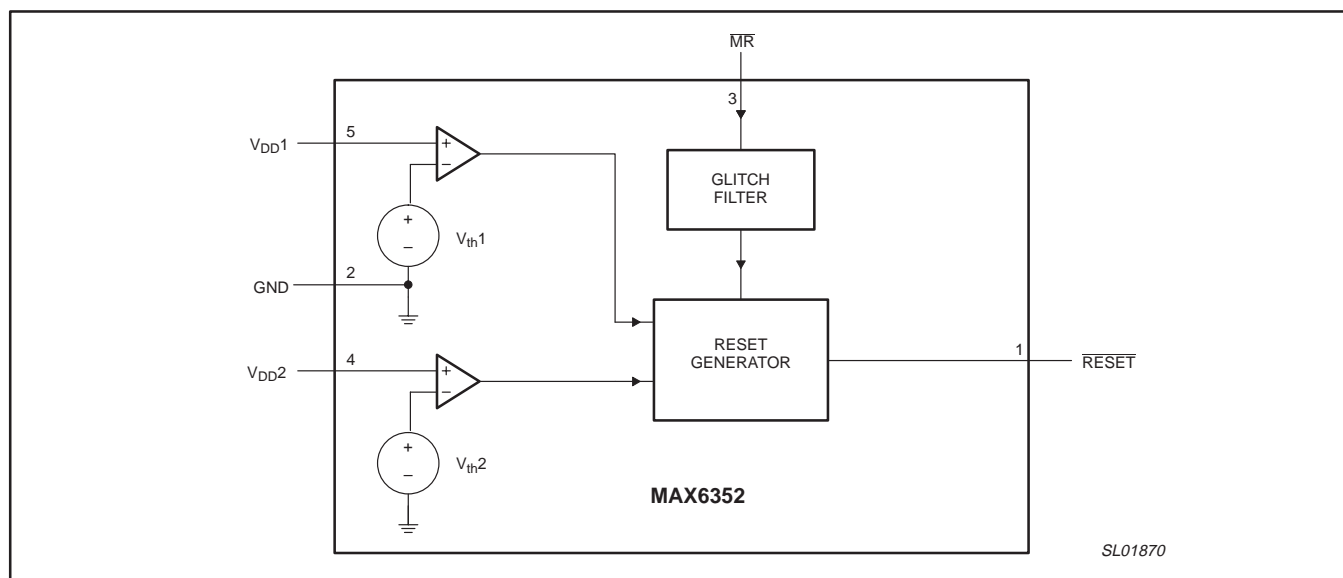


Figure 3. Block diagram.

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TIMING DIAGRAM

The timing diagram in Figure 4 depicts the operation of the device. Letters indicate events on the TIME axis. V_{DD} applies to either V_{DD1} or V_{DD2} .

On power-up, when V_{DD} reaches 1 V, $\overline{\text{RESET}}$ is guaranteed to be a logic LOW.

At Event A, V_{DD} rises to reset threshold voltage, V_{th} . At this time, the internal reset delay timer is initiated. $\overline{\text{RESET}}$ remains asserted for a reset delay time, t_{RP} of typically 180 ms after the supply voltage rises above the reset threshold, V_{th} .

Event B: At this time, the reset is released. $\overline{\text{RESET}}$ goes HIGH. The reset delay time helps to ensure valid reset signals with erratic changes in supply voltage.

Events C–E: At Event C, under brown-out conditions, V_{DD} falls below the reset threshold minus the hysteresis voltage (typically 20 mV), the reset signal is asserted. When power recovers and V_{DD} rises above the reset threshold, it once again initiates the reset

delay timer (Event D). At Event E, V_{DD} falls below the reset threshold before the reset delay time is reached, and reset remains asserted.

At F, the V_{DD} rises above the reset threshold and remains above the reset threshold for typically 180 ms. At G, the reset is once again released.

At H, the $\overline{\text{MR}}$ is externally pulled LOW for greater than 1 μs (minimum $\overline{\text{MR}}$ pulse width, t_{MR} for $V_{DD} = +5\text{ V}$).

At I, the manual reset is asserted in 100 ns (typical $\overline{\text{MR}}$ to reset out delay time, t_{MD} for $V_{CC} = +5\text{ V}$).

At J, the $\overline{\text{MR}}$ pin returns HIGH. At this point, reset delay timer is initiated and in typically 180 ms, (at K), the reset condition is released.

Event L: On power-down, when V_{DD} falls below $V_{th} - 20\text{ mV}$, $\overline{\text{RESET}}$ is guaranteed to be asserted until V_{DD} falls below 1 V.

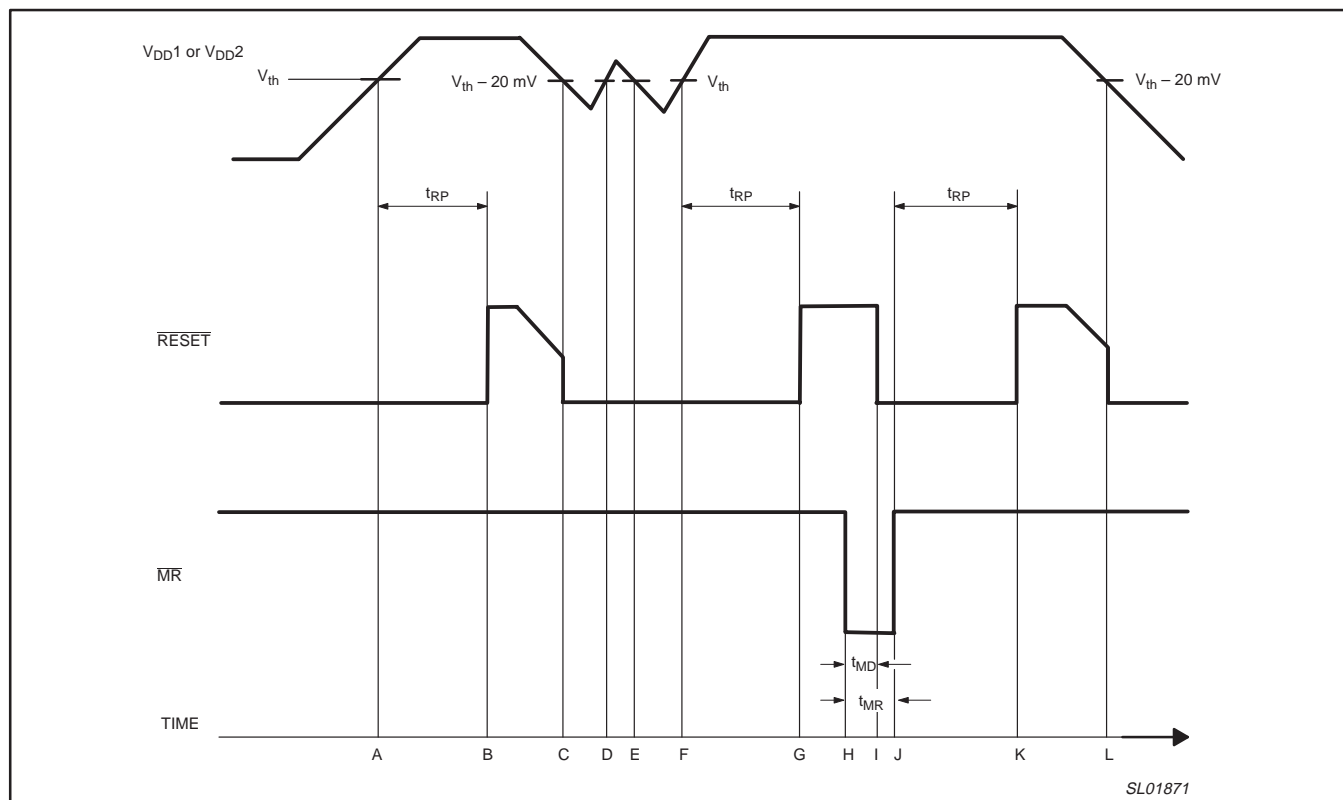


Figure 4. Timing diagram.

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APPLICATION INFORMATION

Negative-going V_{DD} transients

The MAX6352-XX is relatively immune to short duration, negative-going V_{DD} transients or power glitches. This capability greatly reduces false resets with short-duration pulses.

Figure 5, "Maximum V_{DD} transient duration versus reset threshold overdrive", shows the maximum transient condition for which reset signal are not generated. The graph shows the maximum pulse width that a negative-going transient may have before it will generate a reset signal.

Note: As the amplitude of the transient increases, the maximum allowable transient pulse width decreases.



Figure 5. Maximum V_{DD} transient duration versus reset threshold overdrive.

Interfacing to μ Ps with bi-directional RESET pins

The MAX6352-XX RESET output is open drain and is easily interfaced with microprocessors which have bi-directional reset pins, such as the Motorola 68HC11. Directly connecting the MAX6352-XX RESET output to the μ P's reset input and providing a pull-up resistor to V_{DD} allows either device to independently assert reset (Figure 6).

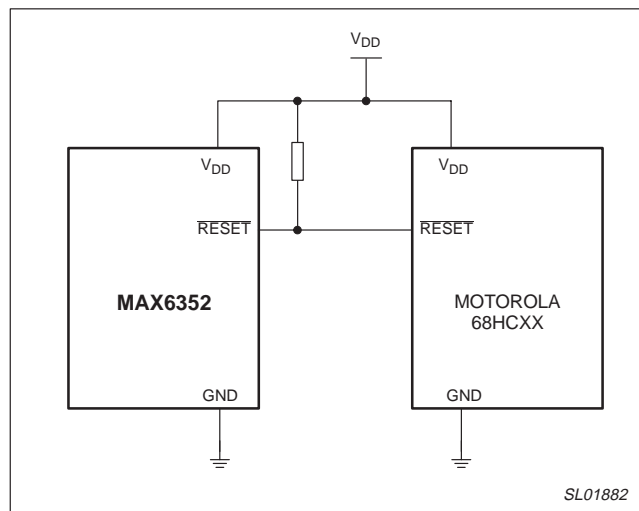


Figure 6. Interfacing to μ Ps with bidirectional reset I/O.

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PACKING METHOD

The MAX6352-XX is packed in reels, as shown in Figure 7.

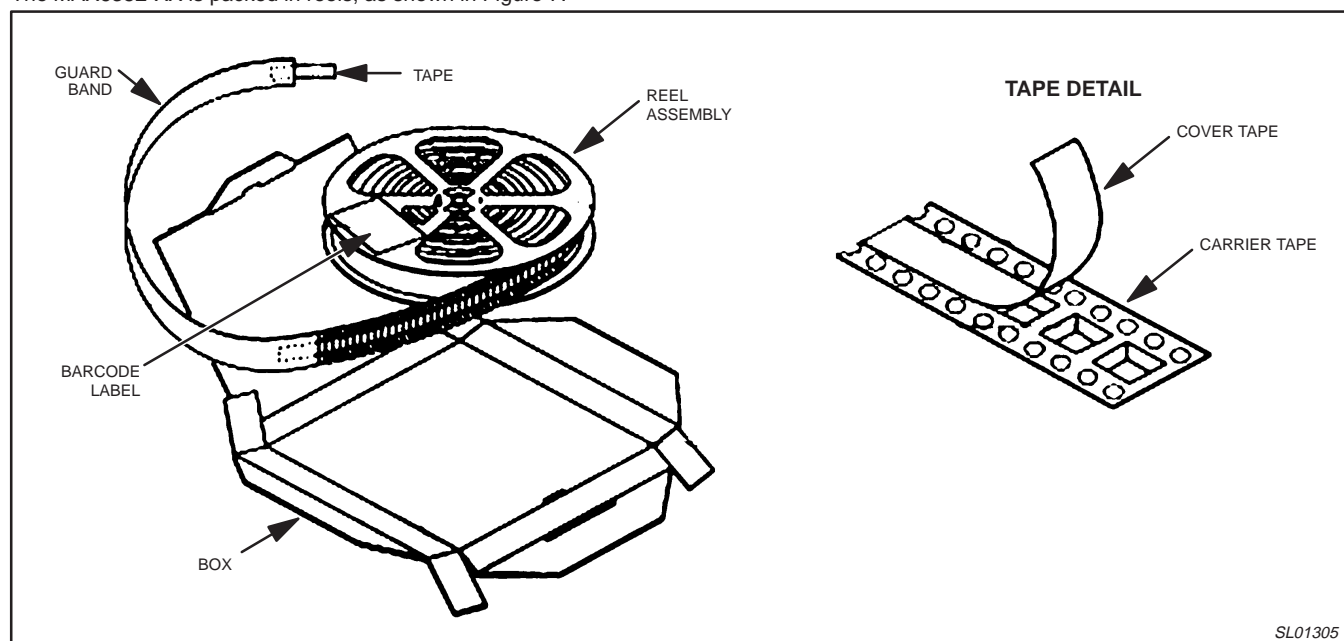


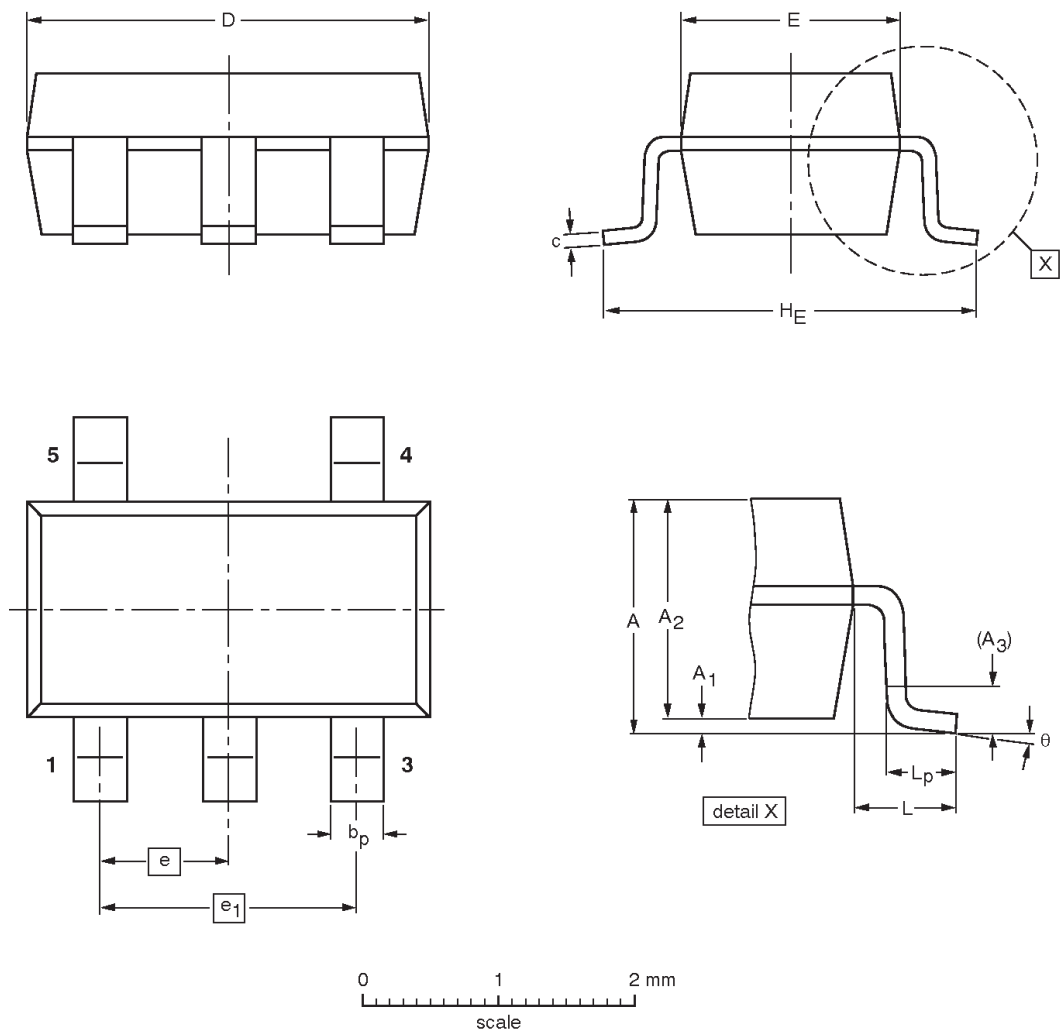
Figure 7. Tape and reel packing method.

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Plastic small outline package; 5 leads; body width 1.6 mm

SOP003



DIMENSIONS (mm are the original dimensions)

| UNIT | A _{max.} | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽²⁾ | e | e ₁ | H _E | L | L _p | θ |
|------|-------------------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|------|----------------|----------------|-----|----------------|----------|
| mm | 1.35 | 0.15 0.05 | 1.2 1.0 | 0.25 | 0.50 0.25 | 0.22 0.08 | 3.0 2.7 | 1.7 1.5 | 0.95 | 1.9 | 3.0 2.6 | 0.6 | 0.55 0.35 | 8° 0° |

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|--------------------|------------|--------|-------|--|------------------------|----------------------|
| | IEC | JEDEC | JEITA | | | |
| SOP003 | | MO-178 | | | | 03-06-25 03-10-07 |

Dual voltage microprocessor supervisory IC

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REVISION HISTORY

| Rev | Date | Description |
|-----|----------|--|
| _2 | 20031016 | Product data (9397 750 12081). ECN 853-2418 30311 dated 08 September 2003. Modifications: <ul style="list-style-type: none"> Figures 1, 3, and 6 modified: change frame/chassis ground to earth ground symbol. Change package outline version to SOP003 in Ordering information table and Package outline sections. |
| _1 | 20030801 | Product data (9397 750 10608). ECN 853-2418 29712 dated 21 March 2003. |

Data sheet status

| Level | Data sheet status ^[1] | Product status ^{[2] [3]} | Definitions |
|-------|----------------------------------|-----------------------------------|--|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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